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A High-Efficiency Ka-Band Active Frequency Doubler MMIC in 150 nm GaN HEMT Technology

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Summary

In this work, the design and electromagnetic (EM) simulation results of an active single-balanced push-push frequency doubler Monolitithic Microwave Integrated Circuit (MMIC) in 150 nm depletion mode Gallium Nitride (GaN) HEMT technology are discussed. The design yields a conversion gain of 7.9 dB with a half-power (3-dB) bandwidth spanning from 27.6 GHz up to 31.2 GHz for an input power of 18.3 dBm. On top of that, the Power-Added Efficiency (PAE) is 20.3% and the harmonic rejection is larger than 35 dB at 30 GHz.

1 Introduction

With the increasing demand for higher data rates in communication systems, a shift to higher frequencies is needed. Specifically with the introduction of 5G Frequency Range 2 (FR2), spanning from 24 GHz up to 54 GHz, compared to 4G, being sub 6 GHz, hardware re-design is necessary. However, high-frequency Voltage-Controlled Oscillator (VCO) design with low phase noise and a wide tuning range is hard to achieve, so frequency multiplication will be critical to alleviate this issue [1].

Literature shows quite some research on frequency doublers in CMOS and Silicon Germanium (SiGe), whereas designs in Gallium Nitride (GaN) are rather scarce. In essence, the most appropriate design for a frequency doubler is the active single-balanced push-push topology, which inherently cancels out odd-order harmonic content due to anti-phase signaling, while even-order harmonic content is enhanced by superposition. This topology is often extended with a cascode to further boost the conversion gain and to minimize the Miller capacitance [2, 3]. As this design is optimized for high-efficiency and not for conversion gain, this has not been implemented. This paper will dive into the design methodology and electromagnetic (EM) simulation results of an active single-balanced push-push frequency doubler Monolithic Microwave Integrated Circuit (MMIC) in 150 nm depletion mode GaN HEMT technology, specifically in the Win Semiconductors NP15-00 process.

2 Design Methodology

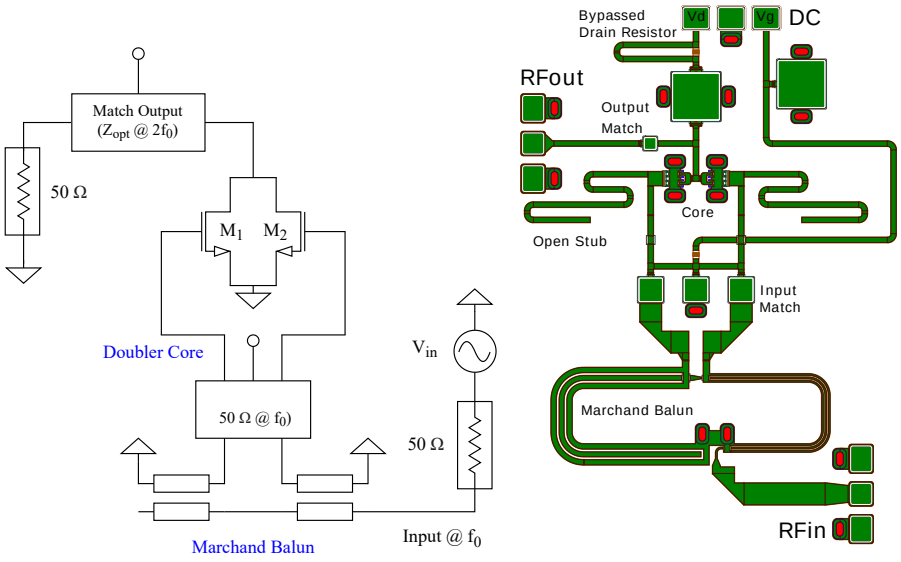
Figure 1 depicts the simplified schematic for the frequency doubler, as well as the MMIC layout. The first challenge is to design a compact Marchand balun at 15 GHz, which is done using a folded structure. Hence, the inner half-wavelength conductor edge couples to the outer quarter-wavelength conductors. The balun has a single-ended input impedance of 50 Ω and a differential output impedance of 100 Ω, together with a phase imbalance smaller than 3° and a loss of only 0.8 dB. The core circuit comprises an active single-balanced push-push topology with transistor sizes of 4×50 μm to be able to carry an output power of at least 25 dBm, while also being capable of producing some conversion gain. On top of that, the transistors are biased in class B to enhance the second order harmonic generation, as well as the efficiency. Moreover, the output matching network is designed to attain the highest output power using harmonic load-pull, yielding an optimum impedance of 5.1 + j27.2 Ω. At the top of the layout, a large bypass capacitor can be seen at the drain line, which is working in conjunction with the bypassed drain resistor to steer the low-frequency resonance of the circuit. After designing the output match, the input matching network is conjugately matched to 50 Ω using a simple series-shunt transmission line section. To prevent leakage of the second harmonic back to the transistor gates, a quarter-wavelength open stub is designed at the second harmonic frequency, being 30 GHz.

3 EM Simulation Results

Prior to extracting the results, the stability of the circuit for bondwire inductances from 0 H up to 10 nH has been checked, alluding to internal closed loop stability. Figure 2a presents the harmonic output power, where it can be seen that the second harmonic is 35.9 dB above the fourth harmonic at 30 GHz. Furthermore, Figure 2b shows a conversion gain of 7.9 dB, a Power-Added Efficiency (PAE) of 20.3%, and a Drain Efficiency (DE) of 24.1% at 30 GHz.

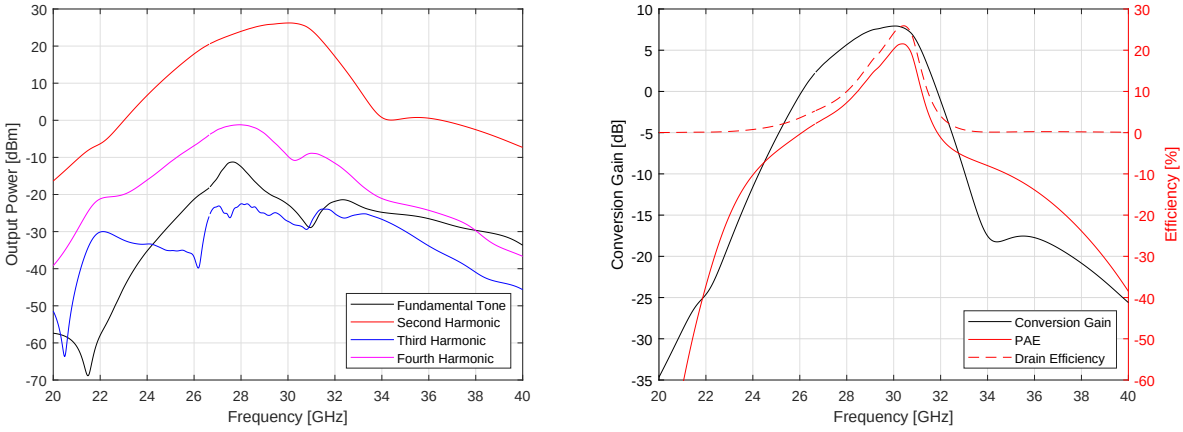
4 Conclusion

An active single-balanced push-push frequency doubler MMIC has been designed in 150 nm depletion mode GaN HEMT technology from 15 GHz to 30 GHz. The EM simulation results show a conversion gain of 7.9 dB with a half-power bandwidth of 3.6 GHz. Lastly, harmonic load-pull was performed, yielding a PAE of 20.3% at 30 GHz for an input power of 18.3 dBm.



(a) Simplified schematic. **(b)** Chip layout.

Figure 1. Simplified schematic and chip layout of the proposed frequency doubler.



(a) Harmonic output power. **(b)** Conversion gain, PAE, and DE.

Figure 2. Simulation results for the harmonic output power, conversion gain, PAE, and DE versus second harmonic frequency (with respect to the fundamental tone) with an input power of 18.3 dBm.

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